AMENDMENT TO SPECIFICATION

Please replace the paragraph beginning at page 2, line 10 with the following replacement paragraph:

-- This application is related to and claims priority benefit under 35 U.S.C. 119(e) of U.S. Provisional patent Application Serial No. 80/243,708, filed October 26, 2000 to Snyder, et al. which is hereby incorporated herein by reference. This application is also related to U.S. Patent Application serial no. 09/893,048, filed June 26, 2001 to Kutz, et al. entitled "Multiple Use of Microcontroller Pad", attorney docket number CYPR-CD00231 which is hereby incorporated herein by reference. --

Please replace the paragraph beginning at page 9, line 12 with the following replacement paragraph:

-- In this embodiment, digital NAND gates are used for switches in the digital signal paths. Other digital gates such as AND gates could also be used. NAND gate 520 is used to gate a signal from digital out 326 to pad 114 through an isolation resistor 526. The pad 114 is configured as a digital output by use of a digital signal applied to digital out enable 530 to either pass or reject digital signals at node 326. A logic zero at 530 effectively forces the output of NAND gate 520 to a logic high state at all times to effectively turn off the gate. Resistor 526 isolates this high state from the pad 114. Other isolation resistor arrangements could also be used. In a similar manner, NAND gate 540 is used to gate a signal from pad 114 to digital in 320

through an isolation resistor ~~546~~ (not shown). The pad 114 is configured as a digital input by use of a digital signal applied to digital in enable 550 to either pass or reject digital signals at pad 114. A logic zero at 550 effectively forces the output of NAND gate 540 to a logic high state at all times. Again, the switching arrangement can be configured under the control of the processor 120 as either analog or digital, input or output. --